

BA25

32-bit
Application Processor

Implements a 32-bit processor for demanding systems running applications on generalpurpose operating systems such as Linux and Android. The high-performance BA25[™] processor runs at high clock frequencies yet has a smaller silicon footprint than most competing application processors (e.g., over 800MHz and from 150Kgates in TSMC65nmLP, 12-track library).

This royalty-free 32-bit processor core is binary-compatible with other members of the silicon-proven BA2x processor family. Its BA2 instruction set is relatively simple and extremely compact, offering system area and energy savings benefits. Programing is facilitated with the included C/C++ tool chain, Eclipse IDE, architectural simulator, and ported C libraries, RTOSs, and OSs.

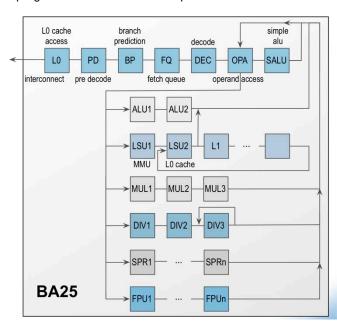
Processor Description

The seven-stage pipelined architecture runs at high frequencies and further enhances performance by supporting out-of-order execution and branch prediction. An optional IEEE 754 compliant floating-point unit accelerates floating point computation.

The BA25 processor uses two-level data and instruction caches—with L0 running at the CPU's clock frequency and L1 running at half that—and a two-level memory management unit. The size and associativity of the caches and MMU are configurable at synthesis time. The system interface uses two AMBA® AXI4 buses, one for data and one for instructions, both of configurable data width. Two tightly-coupled quick memory (QMEM) buses allow fast access for time-critical code and data, and can be used for inter-core communication in a multi-core architecture.

The energy efficiency BA25 enables power management with clock gating and power shut-off of unused units, and through software and hardware control over the clock frequency of the CPU and buses. Wake-up from sleep mode is triggered by an interrupt issued by the embedded tick-timer or by an external source. Rapid interrupt response is facilitated by the embedded programmable vectored interrupt controller.

Block Diagram



Features

High Performance 32-bit CPU

- Seven-Stage Pipeline
- Out-of Order Completion
- Sophisticated Branch Prediction
- Optional Floating Point Unit
- 1.51 DMIPS/MHz
- 2.51 Coremarks/MHz
- 800+ MHz on TSMC 65nm LP

Efficient Power Management

- Dynamic clock gating and power shut-off of unused units
- Software- and hardwarecontrolled clock frequency
- Wake-up on tick timer or external interrupt

Fast & Flexible Memory Access

- Separate Instruction and Data Caches and MMU
 - AXI4 data & instruction buses (32-, 64- or 128-bit) with 4 GBytes direct addressable space on each bus
- Tightly coupled Quick Memory (QMEM) interface for fast and deterministic access to code and/or data

Two-Level Cache and MMU

- L0 cache running at core frequency and L1 cache running at half the core frequency
- 1–16 Kbytes L0 caches, up to four-way set associative
- 32–512 Kbytes L1 caches, up to four-way set associative
- L0 MMU with up to 32 four-way associative entries
- L1 MMU with up to 2048 fourway associative entries

Optional Integrated Peripherals

- Vectored Interrupt Controller
- Microcontroller peripherals such as GPIO, UART, Real-Time Clock, Timers, I2C, and SPI
- Memory controllers, interconnect IP, and more

Easy Software Development

- Non-intrusive JTAG debug/trace for both CPU and system
- Complex chained watchpoint and breakpoint conditions
- BeyondStudio™ complete IDE for Windows or Linux under Eclipse
- Ported libraries and operating systems

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Applications

The royalty-free, high-performance BA25 processor core is suitable as the main system processor in a multitasking environment and is a competitive choice for designs running on full operating systems such as Linux or Android. Target product types include:

- · Set-top boxes and media players,
- · Image and video processing systems, and
- Wireless, battery-powered, or ultra-low-cost devices.

The BA2 Instruction Set

The BA2 instruction set provides extreme code density without compromises on performance, ease of use, or scalability. It features:

- A linear, 32-bit address space
- Variable length instructions: 16, 24, 32, or 48 bits
- · Simple memory addressing modes
- A configurable number of 12 to 32 general purpose registers
- Efficient flow-control, arithmetic, and load/store instructions
- · Floating point and DSP extensions

Customizable Platforms

The BA25 processor can be delivered pre-integrated with typical microcontroller peripherals such us UARTs, timers and serial communication cores, or with memory controllers and interconnect IP cores. Contact CAST Sales for details

Support and Services

The core as delivered is warranted against defects for 90 days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

IP Integration Services are also available to help minimize time to market for BA25-based systems.

Deliverables

The core is available for ASICs in synthesizable Verilog source code, and includes everything required for successful implementation. The core is delivered with software development tools Windows and Linux, with an Eclipse IDE interface.

Related Products

The BA2x[™] Processor Family includes a set of royalty-free, pre-configured products intended for different applications:

- BA22-AP 32-bit Basic Application Processor, for embedded applications that may need to run a full OS.
- BA22-CE 32-bit Cache-Enabled Embedded Processor, for deeply embedded systems using off-chip instruction and data memories and possibly running an RTOS; 5-stage pipeline, caches but no MMU.
- BA22-DE 32-bit Deeply Embedded Processor, for deeply embedded applications that use on-chip instruction and data memories.
- BA21 32-bit Low-Power Deeply Embedded Processor, implements a 32-bit low-power processor that delivers better performance than most processors of its size.

Platforms

- BA2x-AXI-PP Pre-integrated peripherals platform for the AMBA3 AXI bus.
- BA2x-AHB-PP Pre-integrated peripherals platform for the AMBA2 AHB/APB buses.







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