C8237

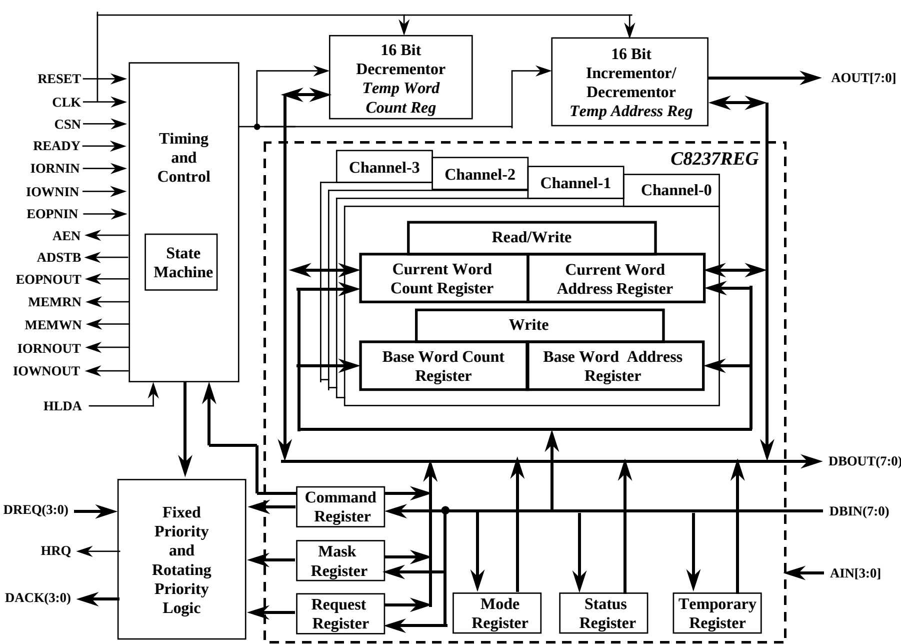
Programmable DMA Controller Core

The C8237 Programmable DMA Controller core (C8237 core) is a peripheral interface circuit for microprocessor systems. The core is designed for use with an external, 8-bit address latch. It contains four independent channels and may be expanded to any number or channels by cascading additional controller chips. Each channel has a full 64K address and word count capability.

Applications

The C8237 core is designed to improve system performance by allowing external devices to directly transfer information from the system memory.

Block Diagram



Features

- Enable/Disable control of individual DMA requests
- Four, independent DMA channels
- Independent auto-initialization of all channels
- Memory-to-Memory transfers
- Memory block initialization
- Address increment or decrement
- Directly expandable to any number of channels
- End of process input for terminating transfers
- Software DMA requests
- Independent polarity control for DREQ and DACK signals
- The C8237 was developed in HDL and synthesizes to approximately 5,500 gates depending on the technology used.
- Functionality based on the Intel 8237

Functional Description

The C8237 core is partitioned into modules as shown in the block diagram and described below:

Timing & Control

It generates internal timing and external control signals for the C8237. The timing Control block derives internal timing from the clock input. The C8237 operates in two major cycles, idle cycle (Si) and Active cycle (S0, S1, S2, S3, and S4). Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. It requires eight states for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from –memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer. Each state is composed of one full clock period.

Fixed Priority & Rotating Priority Logic

The Fixed Priority fixes the channels in priority order based upon the descending value of their number. The lowest priority channel is 3 and the highest priority channel is 0.

With Rotating Priority, the last channel to get service becomes the lowest priority channel with the others rotating accordingly.

C8237 Registers

The C8237 contains 344 bits of internal memory in the form of registers. CSN must be low when the microprocessor is attempting to write or read the internal registers of the C8237.

Command Register

Write Command Register Command:

A3	A2	A1	A0	IORN	IOWN
1	0	0	0	1	0

This 8-bit register controls the operation of the C8237. It is programmed by the microprocessor and is cleared by Reset or a Master Clear instruction.

D7	D6	D5	D4	D3	D2	D1	D0

Bit0: 0 -> Memory-to-memory disable
1 -> Memory-to-memory enable

Bit1: 0 -> Channel 0 address hold disable
1 -> Channel 0 address hold enable
X -> if bit0 = 0

Bit2: 0 -> Controller enable
1 -> Controller disable

Bit3: 0 -> Normal timing
1 -> Compressed timing
X -> if bit 0 = 1

Bit4: 0 -> Fixed priority
1 -> Rotating priority

Bit5: 0 -> Late write
1 -> Extended write
X -> if bit3 = 1

Bit6: 0 -> DREQ sense active high
1 -> DREQ sense active low

Bit7: 0 -> DACK sense active low
1 -> DACK sense active high

Mode Register

Write Mode Register Command:

A3	A2	A1	A0	IORN	IOWN
1	0	1	1	1	0

Each channel has a 6-bit Mode register. It is programmed by the microprocessor.

D7	D6	D5	D4	D3	D2	D1	D0

Bit1 & Bit0: 00 -> Channel 0
01 -> Channel 1
10 -> Channel 2
11 -> Channel 3

Bit3 & Bit2: 00 -> Verify transfer (pseudo transfer)
01 -> Write transfer (from I/O to the memory)
10 -> Read transfer (from the memory to I/O)
11 -> Illegal
XX -> if bits 6 and 7 = 11

Bit4: 0 -> Auto initialization disable
1 -> Auto initialization enable

Bit5: 0 -> Address increment select
1 -> Address decrement select

Bit7 & Bit6: 00 -> Demand mode
01 -> Single mode
10 -> Block mode
11 -> Cascade mode

Demand Transfer Mode: The device will continue making transfers until a TC or external EOPN is encountered or until DREQ goes inactive.

Single Transfer Mode: The device makes one transfer only. DREQ must be held active until DACK becomes active in order to be recognized.

Block Transfer Mode: The device is active by DREQ or software request to continue making transfers during the service until a TC or an external EOPN is encountered. DREQ need only be held active until DACK becomes active.

Cascade Transfer Mode: This mode is used to cascade more than one C8237 together for simple system expansion. The ready input is ignored in this cascade transfer mode.

Request Register

Write Request Register Command:

A3	A2	A1	A0	IORN	IOWN
1	0	0	1	1	0

Each channel has a request bit associated with it in the 4-bit Request register. These are non-maskable and subject to prioritization by the Priority Encoder. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOPN. The entire register is cleared by a Reset. In order to make a software request, the channel must be in Block Mode.

X	X	X	X	X	D2	D1	D0

Bit1 & Bit0: 00 -> Channel 0

01 -> Channel 1

10 -> Channel 2

11 -> Channel 3

Bit2: 0 -> Reset request bit

1 -> Set request bit

Mask Register

Each channel has a mask bit associated with it which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOPN if the channel is not programmed for Auto initialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur.

Programming All Mask Register Bits:

Write All Mask Register Bits Command:

A3	A2	A1	A0	IORN	IOWN
1	1	1	1	1	0

X	X	X	X	X	D2	D1	D0

Bit1 & Bit0: 00 -> Channel 0

01 -> Channel 1

10 -> Channel 2

11 -> Channel 3

Bit2: 0 -> Clear mask bit

1 -> Set mask bit

Programming Single Mask Register Bits:

Write Single Mask Register Bit Command:

A3	A2	A1	A0	IORN	IOWN
1	0	1	0	1	0

X	X	X	X	D3	D2	D1	D0

Bit0: 0 -> Clear channel 0 mask bit

1 -> Set channel 0 mask bit

Bit1: 0 -> Clear channel 1 mask bit

1 -> Set channel 1 mask bit

Bit2: 0 -> Clear channel 2-mask bit

1 -> Set channel 2 mask bit

Bit3: 0 -> Clear channel 3-mask bit

1 -> Set channel 3 mask bit

Status Register

Read Status Register Command:

A3	A2	A1	A0	IORN	IOWN
1	0	0	0	0	1

This register is available to be read out of the C8237 by the microprocessor. It contains information about the status of the devices at this point. Bits 0-3 are set when that channel reaches a TC or an external EOPN is applied. These bits are cleared upon Reset and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting.

D7	D6	D5	D4	D3	D2	D1	D0

Bit0: 1 -> Channel 0 has reached TC

Bit1: 1 -> Channel 1 has reached TC

Bit2: 1 -> Channel 2 has reached TC

Bit3: 1 -> Channel 3 has reached TC

Bit4: 1 -> Channel 0 request

Bit5: 1 -> Channel 1 request

Bit6: 1 -> Channel 2 request

Bit7: 1 -> Channel 3 request

Temporary Register

Read Temporary Register Command:

A3	A2	A1	A0	IORN	IOWN
1	1	0	1	0	1

This register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor. The temporary register is cleared by a Reset.

Current Address Register

Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor.

Current Word Register

Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The word count is decremented after each transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read by the microprocessor in the Program Condition.

Base Address and Base Word Count Registers

Each channel has a 16-bit Base Address and 16-bit Base Word Count register. These registers store the original value, which will be loaded to current registers during Auto initialize.

Word Count and Address Register Command Codes

Write -> CSN = 0, IORN = 1 and IOWN = 0

Read -> CSN = 0, IORN = 0 and IOWN = 1

Register	A3	A2	A1	A0	FF	DB0-DB7
CH 0 Base and Current Address	0	0	0	0	0	A0-A7
					1	A8-A15
CH 0 Base and Current Word Count	0	0	0	1	0	W0-W7
					1	W8-W15
CH 1 Base and Current Address	0	0	1	0	0	A0-A7
					1	A8-A15
CH 1 Base and Current Word Count	0	0	1	1	0	W0-W7
					1	W8-W15
CH 2 Base and Current Address	0	1	0	0	0	A0-A7
					1	A8-A15
CH 2 Base and Current Word Count	0	1	0	1	0	W0-W7
					1	W8-W15
CH 3 Base and Current Address	0	1	1	0	0	A0-A7
					1	A8-A15
CH 3 Base and Current Word Count	0	1	1	1	0	W0-W7
					1	W8-W15

Software Commands

These three commands do not depend on any specific bit pattern on the data bus.

Clear First/Last Flip-Flop Command:

A3	A2	A1	A0	IORN	IOWN
1	1	0	0	1	0

This command must be executed prior to writing or reading new address or word count information to the C8237.

Master Clear Command:

A3	A2	A1	A0	IORN	IOWN
1	1	0	1	1	0

This command has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The C8237 will be in the idle cycle.

Clear Mask Register Command:

A3	A2	A1	A0	IORN	IOWN
1	1	1	0	1	0

This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Temporary Word Count Register (16 Bit Decrementor)

It will decrement the word count after each transfer. When the value in the register goes from zero to FFFFH, a Terminal Count (TC) will be generated.

Temporary Address Register (16 Bit Incrementor/Decrementor)

Base on the mode of the address, the address will be decremented or incremented after each transfer. And the intermediate values of the address are stored in the Current Address register during the transfer.

Implementation Results

The following are typical performance and utilization results using a variety of implementation technologies.

ASIC Library	Gate Count		Performance (MHz)
UMC 0.18	5,500		253 MHz
Altera	**LEs**	**Memory**	**Performance (MHz)**
Cyclone EP1C20-6	1,007	0	97
Stratix EP1S20-5	1,007	0	94
Stratix-II EP2S60-3	816	0	140
Xilinx	**Slices**	**Memory**	**Performance (MHz)**
Spartan-3 XC3S200-4	469	0	50
Virtex-II XC2V100-6	397	0	97
Virtex-II Pro XC2VP2-7	397	0	103

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core includes everything required for successful implementation:

RTL Source Licenses

- VHDL or Verilog source code
- Testbench
- Wrapper for matching the I/O of the original device
- Vectors for testbench
- Expected results for testbench
- Simulation script
- Synthesis script

Netlist Licenses

- Post-synthesis gate-level netlist
- Testbench
- Vectors for testbench
- Expected results for testbench
- Wrapper for matching the I/O of the original device
- Simulation script
- Place & Route script

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